CLAIMS

1. A method for forming an asymmetric-area memory cell, the method comprising:

forming a bottom electrode having an area;

forming a colossal magnetoresistance (CMR) memory film overlying the bottom electrode, having an asymmetric area; and,

forming a top electrode having an area, less than the bottom electrode area, overlying the CMR film.

2. The method of claim 1 wherein forming a CMR film with an asymmetric area includes forming a CMR film with a first area adjacent the top electrode and a second area, greater than the first area, adjacent the bottom electrode.

3. The method of claim 2 wherein forming a CMR film with an asymmetric area includes forming a CMR film first area approximately equal to the top electrode area.

4. The method of claim 3 wherein forming a CMR film with an asymmetric area includes forming a CMR film second area less than the bottom electrode area.

5. The method of claim 3 further comprising:

isotropically depositing a bottom electrode layer;

isotropically depositing a CMR film layer, having a first thickness, overlying the bottom electrode layer;

isotropically depositing a top electrode layer overlying the CMR film layer; and,

wherein forming the top electrode area and the CMR film first area includes etching the top electrode layer and a second thickness portion of the CMR film layer.

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6 ~~5~~. The method of claim 4 further comprising:

forming a first set of sidewall insulators adjacent the top electrode and the second thickness portion of the CMR film; and,

wherein forming a CMR film second area includes etching the remaining portion of the CMR film layer, leaving a third thickness portion of the CMR film second area underlying the first set of sidewall insulators, where the third thickness is equal to the first thickness minus the second thickness.

7 ~~6~~. The method of claim 5 further comprising:

forming a second set of sidewall insulators overlaying the first set of sidewall insulators and adjacent the third thickness portion of the CMR film;

wherein forming a bottom electrode having an area includes etching the bottom electrode layer, leaving a bottom electrode area underlying the first and second set of sidewall insulators.

8 ~~7~~. The method of claim 5 wherein leaving a third thickness portion of the CMR film second area includes leaving a third thickness in the range of 20 to 80% of the first thickness.

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~~8~~. The method of claim 6 wherein forming a first set of sidewall insulators adjacent the top electrode and the second thickness portion of the CMR film includes forming sidewall insulators from a material selected from the group including silicon nitride and aluminum oxide, having a thickness in the range of 50 to 200 nanometers (nm).

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~~9~~. The method of claim 8 wherein forming a second set of sidewall insulators overlaying the first set of sidewalls and adjacent the third thickness portion of the CMR film includes forming sidewall insulators from a material selected from the group including silicon nitride and aluminum oxide, having a thickness in the range of 20 to 100 nm.

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~~10~~. The method of claim 1 wherein forming a bottom electrode includes forming an electrode from a material selected from the group including TiN/Ti, Pt/TiN/Ti, In/TiN/Ti, PtRhOx compounds, and PtIrOx compounds; and,

wherein forming a top electrode includes forming an electrode from a material selected from the group including TiN, TiN/Pt, TiN/In, PtRhOx, and PtIrOx compounds.

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~~11~~. The method of claim 1 wherein forming a CMR memory film overlying the bottom electrode includes forming a $Pr_{0.3}Ca_{0.7}MnO_3$ (PCMO) memory film.

13 ~~12~~. The method of claim 1 wherein forming a CMR memory film overlying the bottom electrode, having an asymmetric area, includes forming a CMR film first thickness in the range of 50 to 350 nanometers.

14 ~~13~~. A method for forming an RRAM asymmetric-area memory cell, the method comprising:

forming a CMOS transistor with source and drain active regions;

forming a metal interlevel interconnect to a transistor active region;

forming a bottom electrode having an area overlying the interlevel interconnect;

forming a colossal magnetoresistance (CMR) memory film overlying the bottom electrode, having an asymmetric area; and,

forming a top electrode having an area, less than the bottom electrode area, overlying the CMR film.

15 ~~14~~. A method for programming an asymmetric-area memory cell using bipolar and uni-polar pulses, the method comprising:

applying a first voltage pulse with a first polarity to a memory cell top electrode;

in response to the first pulse, creating a low resistance in an asymmetrical-area colossal magnetoresistance (CMR) memory film;

applying a second voltage pulse with a second polarity, opposite of the first polarity, to the memory cell top electrode; and,

in response to the second pulse, creating a high resistance in the asymmetric-area CMR memory film;

applying a third pulse, having the same polarity as the second pulse, and a pulse width of greater than 1 microsecond; and,

in response to the third pulse, creating a low resistance in the CMR memory film.

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~~15~~. The method of claim 14 wherein creating a low resistance in the CMR memory film in response to the first pulse includes creating a low resistance in a narrow-area region of the asymmetric-area CMR memory film; and,

wherein creating a high resistance in the CMR memory film in response to the second pulse includes creating a high resistance in the narrow-area region of the asymmetric-area CMR memory film.

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~~16~~. The method of claim 15 wherein creating a low resistance in the CMR memory film in response to the first pulse includes creating a resistance in the range of 1000 to 10k ohms; and,

wherein creating a high resistance in the CMR memory film in response to the second pulse includes creating a resistance in the range of 100k to 10M ohms.

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~~17~~. The method of claim 16 wherein applying a first pulse with a first polarity to the memory cell top electrode includes applying a voltage pulse with a width in the range of 5 to 500 nanoseconds (ns); and,

wherein applying a second pulse with a second polarity to the memory cell top electrode includes applying a voltage pulse with a width in the range of 5 to 500 ns.

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~~18~~. The method of claim 17 wherein the CMR film has a thickness in the range of 50 to 350 nanometers; and,

wherein applying a first pulse with a first polarity to the memory cell top electrode includes applying a pulse with a voltage amplitude in the range of 2 to 6 volts; and,

wherein applying a second pulse with a second polarity to the memory cell top electrode includes applying a pulse with a voltage amplitude in the range of 2 to 6 volts.

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~~19~~. The method of claim 15 wherein includes creating a low resistance in a narrow-area region of the asymmetric-area CMR memory film in response to the first pulse includes creating a low resistance in response to a first electric field in the narrow-area region of the CMR memory film, and a second electric field, with a field intensity less than the first field, in a wide-area region of the CMR memory film; and,

wherein includes creating a high resistance in a narrow-area region of the asymmetric-area CMR memory film in response to the second pulse includes creating a high resistance in response to a third electric field in the narrow-area region of the CMR memory film, opposite in polarity to the first field, and a fourth electric field, with a field

intensity less than the third field, in a wide-area region of the CMR memory film.

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~~20~~. The method of claim 15 wherein applying a first pulse with a first polarity to the memory cell top electrode includes applying a positive polarity pulse;

wherein creating a low resistance in a narrow-area region of the asymmetric-area CMR memory film includes creating a low resistance in a narrow-area region adjacent the top electrode;

wherein applying a second pulse with a second polarity to the memory cell top electrode includes applying a negative polarity pulse; and,

wherein creating a high resistance in a narrow-area region of the asymmetric-area CMR memory film includes creating a high resistance in a narrow-area region adjacent the top electrode.

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~~21~~. An asymmetric-area memory cell comprising:

a bottom electrode having an area;

a colossal magnetoresistance (CMR) memory film overlying the bottom electrode, having an asymmetric area; and,

a top electrode having an area, less than the bottom electrode area, overlying the CMR film.

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~~22~~. The memory cell of claim 21 wherein a CMR film has a first area adjacent the top electrode and a second area, greater than the first area, adjacent the bottom electrode.

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~~23~~. The memory cell of claim 22 wherein the CMR film first area is approximately equal to the top electrode area.

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~~24~~. The memory cell of claim 23 wherein the CMR film second area is less than the bottom electrode area.

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~~25~~. The memory cell of claim 24 wherein the CMR memory film has an overall first thickness, a second thickness portion with the first area, and a third thickness portion with the second area underlying the second thickness portion, where the third thickness is equal to the first thickness minus the second thickness.

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~~26~~. The memory cell of claim 25 further comprising:

a first set of sidewall insulators adjacent the top electrode and the second thickness portion of the CMR film; and,

a second set of sidewall insulators overlaying the first set of sidewall insulators and adjacent the third thickness portion of the CMR film.

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~~27~~. The memory cell of claim 26 wherein the CMR film third thickness in the range of 20 to 80% of the first thickness.

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~~28~~. The memory cell of claim 25 wherein the CMR film first thickness is in the range of 50 to 350 nanometers.

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~~29~~. The memory cell of claim 26 wherein the first set of sidewall insulators is formed from a material selected from the group including silicon nitride and aluminum oxide, each sidewall having a thickness in the range of 50 to 200 nanometers (nm).

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~~30~~. The memory cell of claim 29 wherein the second set of sidewall insulators is formed from a material selected from the group including silicon nitride and aluminum oxide, each sidewall having a thickness in the range of 20 to 100 nm.

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~~31~~. The memory cell of claim 21 wherein the bottom electrode is formed from a material selected from the group including TiN/Ti, Pt/TiN/Ti, In/TiN/Ti, PtRhOx compounds, and PtIrOx compounds; and,

wherein the top electrode is formed from a material selected from the group including TiN, TiN/Pt, TiN/In, PtRhOx compounds, and PtIrOx compounds.

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~~32~~. The memory cell of claim 21 wherein the CMR memory film is formed from $Pr_{0.3}Ca_{0.7}MnO_3$ (PCMO).

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~~33~~. An RRAM asymmetric-area memory cell comprising:

a CMOS transistor with source and drain active regions;

a metal interlevel interconnect overlying a transistor active region;

a bottom electrode having an area, overlying the interlevel interconnect;

a colossal magnetoresistance (CMR) memory film overlying the bottom electrode, having an asymmetric area; and,

a top electrode having an area, less than the bottom electrode area, overlying the CMR film.